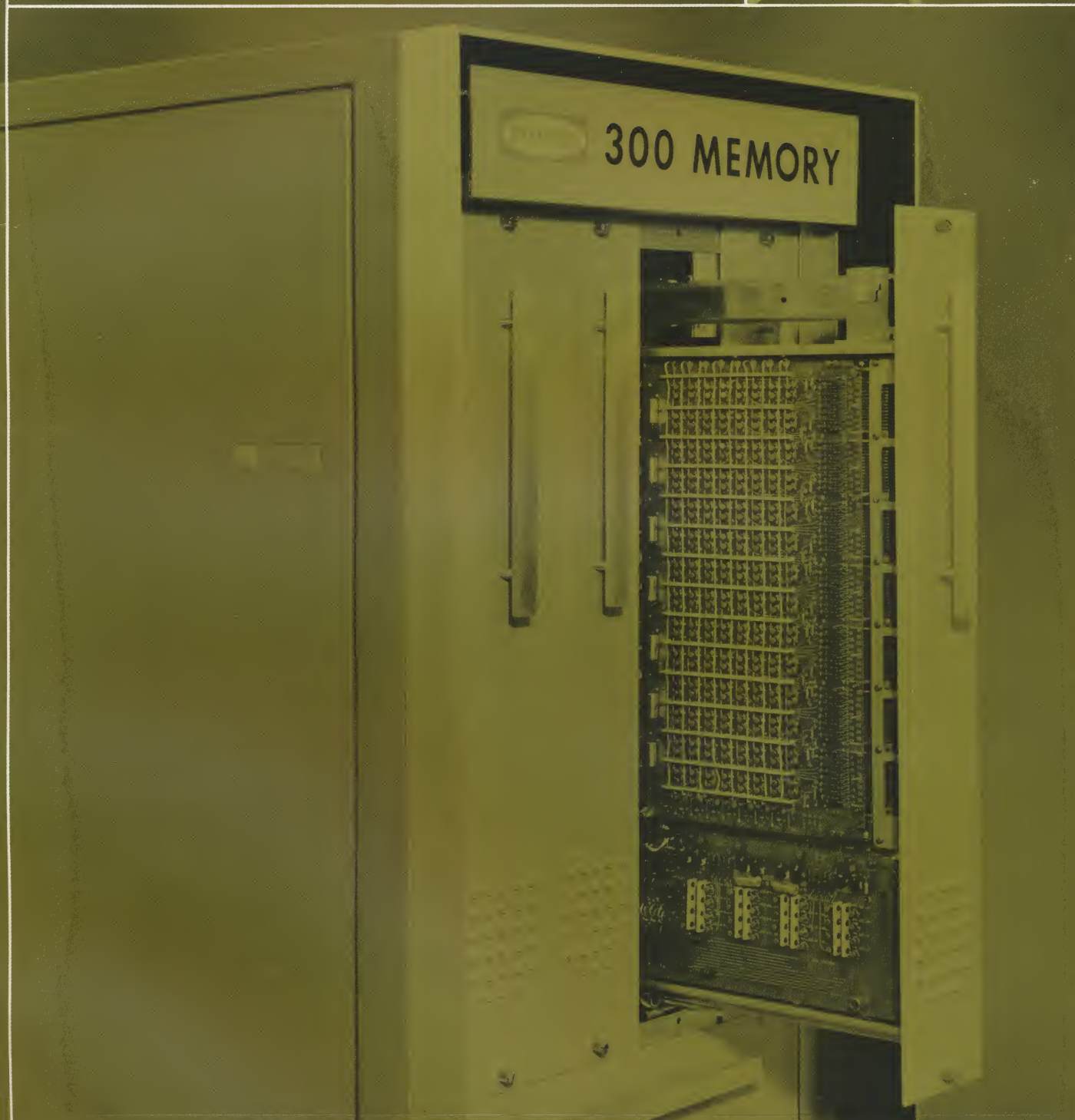


RAYTHEON COMPUTER

300 MEMORY SYSTEM



RAYTHEON COMPUTER • 2700 SO. FAIRVIEW ST., SANTA ANA, CALIFORNIA 92704 (714) 546-7160 TWX 714 546-0444

RAYTHEON

Raytheon Computer now offers a completely new line of read/write random access magnetic core memory systems for computer and data systems applications. Designated the Model 300 series, this new memory provides 900 nanoseconds full cycle time performance using 30 mil cores. Faster cycle times approaching 600 nanoseconds will be available in the same basic memory with 20 mil or smaller cores.

Particular emphasis has been placed on the cost/size/performance characteristics of the new Raytheon 300 Memory. The design utilizes the advantages of "2½D" memory organization and integrated circuits in certain of the electronics to achieve a significant advancement in reliability and operating margins.

Major 300 Memory system features include:

- Low Cost
- High Performance
- Large Capacity
- High Reliability
- Built-in Self-test

Systems are delivered complete with address and data registers, power supplies, power cables and input/output mating connectors.

PERFORMANCE

Raytheon Computer's new 300 Memory series gives the computer and data systems designer a fast, flexible and highly reliable system for main working memory and buffer applications.

The 300 Memory has an access time of 300 nanoseconds to any word location with a read-restore or clear-write cycle completed in 900 nanoseconds.

Standard modules of the 300 Memory are 8192 words with word lengths up to 112 bits and 16,384 words with word lengths up to 56 bits. The design of the 300 Series Memories is based on a modular stack concept, and other word-bit configurations can be supplied as "modified standard" with total storage capacity approaching one million bits. Power supplies and address decoding, timing, writing, reading and sensing electronics are packaged for mounting in a standard 19-inch relay rack.

MEMORY OPERATION

The Raytheon 300 Memory has three separate modes of operation:

1. Clear/Write
2. Read/Restore
3. Split Cycle

The split cycle is a read/modify/write operation in which read timing occurs normally, but writing

is withheld until a write command is generated after the contents of the data register have been modified.

MEMORY SELF-TEST

A self-test capability is built into the 300 Memory to provide an error check on the system without any external signal requirements. The more significant patterns such as all "ones", all "zeros", worst case and worst case complement are generated within the memory system and verified in the read mode at maximum operating speed.

In error-halt mode, data in error is displayed along with address mode. The self-tester can exercise the memory in place by simulating operating conditions. In addition to isolating internal memory problems, the tester may be useful in diagnosing problems external to the memory.

THE 2½D CONCEPT

The "2½D" stack and electronics configuration in the new Raytheon 300 Memory offers an optimum cost approach to realizing microsecond and faster cycle times in toroid core memories with capacities of 8192 words and larger.

In "2½D", a number of 64x64 core matrices (up to 36 per side) are loomed integrally and mounted on a single plane. Costs are substantially reduced and overall system reliability is significantly enhanced by the elimination of the typical X-Y soldered connections around each core matrix. Another major cost saving is realized by the elimination of the inhibit winding. Only three windings total are required in "2½D" memories.

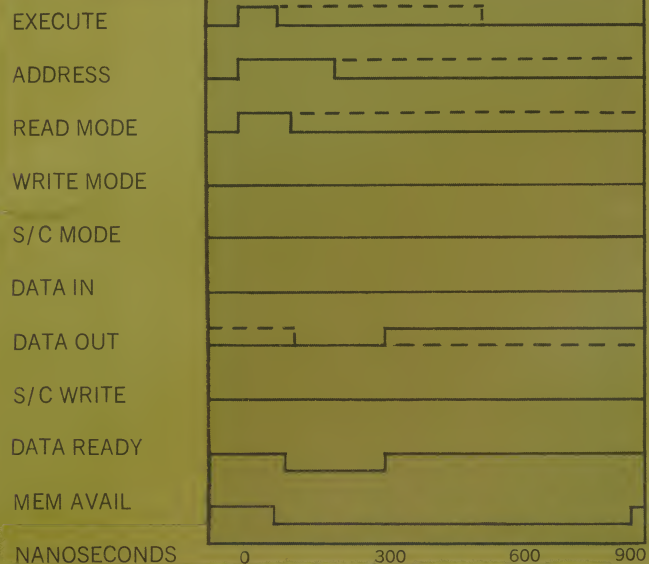
Electronics for "2½D" drivers have also been reduced in cost. Drive lines are shorter than 3D systems—the largest being 768 bits in a typical 16,384-word by 24-bit system. Low cost, low voltage transistors can thus be used with the added speed advantage of faster settling times.

In performance, "2½D" organization offers a tangible breakthrough in achieving low cost 500 nanosecond memory systems. Elimination of the inhibit winding makes possible faster memory cycling since internal timing delays can be shortened.

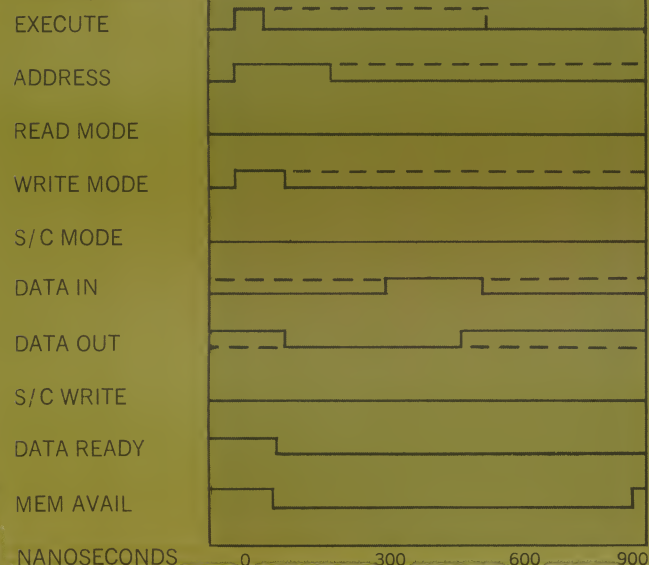
Using 30 mil cores, now in full scale production, systems with 900 nanosecond cycle times and wide operating margins are readily available. By substituting 20 mil cores, cycle time performance can be improved to approximately 600 to 650 nanoseconds. Such systems will be available on a production basis in mid-1967.

SYSTEM TIMING

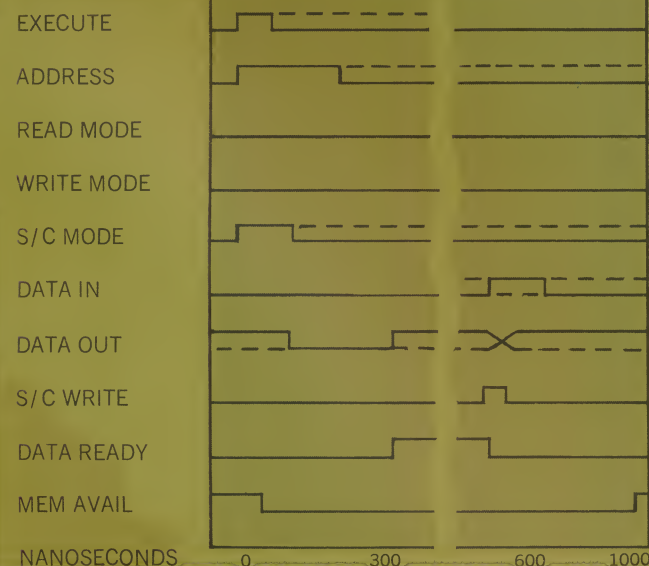
READ/RESTORE



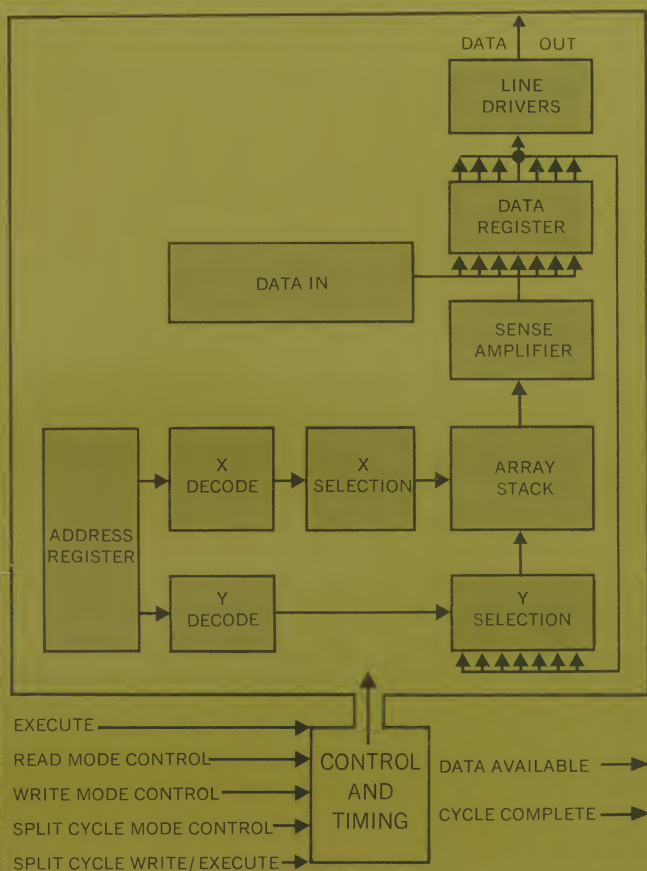
CLEAR/WRITE



SPLIT CYCLE



SYSTEM BLOCK DIAGRAM



RAYTHEON 300 MEMORY SYSTEM

SPECIFICATIONS	MEMORY INTERFACE
GENERAL Systems are supplied complete including address and data registers, built-in self-test unit, and power supply. SYSTEM ORGANIZATION 2½D. SEMICONDUCTORS All-silicon. SIZES 8192 words of up to 112 bits (standard module). 16,384 words of up to 56 bits (standard module). Modified standard modules are available in other word/bit configurations with total bit capacities approaching one million bits. OPERATING MODES & CYCLE TIMES Clear/Write — 900 nanoseconds. Read/Restore — 900 nanoseconds. Split Cycle — 1000 nanoseconds. ACCESS TIME 300 nanoseconds. TEMPERATURE RANGE Operating +10°C to +40°C ambient. Non-operating -40°C to +70°C. HUMIDITY 90% RH with no condensation. SHOCK & VIBRATION Designed for operation in commercial ground environment. Will withstand shipment via air/rail/truck/ship transportation in proper shipping container. MOUNTING Designed for mounting in standard 19" rack. Overall dimensions: Memory — Height 48" Depth 15½" Power Supply — Height 14½" Depth 18" WEIGHT Approximately 350 lbs. POWER REQUIREMENT 105 - 125 VAC 60 cps three-wire single phase (standard supply). Options available: —50, 60, or 400 cycles in either single phase or three phase.	INPUT <i>Read Mode Control Level</i> — when true, the memory will perform a Read/Restore cycle. <i>Write Mode Control Level</i> — when true, the memory will perform a Clear Write cycle. <i>Split Cycle Mode Control Level</i> — when true, the memory will perform a Split Cycle. <i>Address Input</i> — binary coded designation of memory storage location. <i>Data Input</i> — binary coded data to be written into the memory. <i>Execute</i> — pulse initiates one memory cycle of the mode established by mode control lines. <i>Split Cycle Write Execute</i> — starts the Write operation of a Split Cycle. LOGIC LEVELS The memory provides termination for single-ended, twisted pair transmission line. Logic "One" — a voltage level between +2.5 and +5.0 volts Logic "Zero" — a voltage level between 0 and +1.0 volts. OUTPUT <i>Data Out</i> — binary coded data read out of memory. <i>Cycle Complete</i> — true level indicates that the selected memory cycle is finished and memory is available for recycling or new mode selection. <i>Data Available</i> — true output indicates that memory read operation has been completed and a data word is available in the data register. SIGNAL CHARACTERISTICS The memory is designed to drive a single ended, twisted pair transmission line terminated in its characteristic impedance to a positive supply voltage at the receiving end. This line is driven by an NPN transistor (emitter-to-ground) which is on for logic "zero" and off for logic "one". This transistor will sink a maximum of 40ma at no more than 0.6 volt in "zero" state. Transistor will withstand up to 6 volts in "one" state.

Raytheon Computer also manufactures BIAX® and MicroBIAX® non-destructive readout memories for aerospace, military, industrial and commercial use. For more information, contact Manager, Memory Products at the address given below:

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